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**Sukkur IBA University** Department of Electrical Engineering ESE-211: Digital Logic Design Lab

## IV-Semester Project

**Digital Clock using gates**

Instructor: Dr.-Ing. Kashif Hussain

# Introduction

This lab report documents the design and implementation of a digital clock using basic logic gates and Flip Flops. The project is a part of the Digital Electronics course and aims to provide practical experience in using combinational and sequential logic circuits to develop functional digital systems.

# Objectives

* To design a digital clock using basic logic gates.
* To understand the working of combinational and sequential circuits.
* To gain hands-on experience in circuit design and troubleshooting.

# Components Used

* Logic Gates: AND, OR, NOT.
* Flip-Flops: JK Flip-Flops.
* Digital Clock to generate 1 Hz clock pulse
* Counters (Mod-10 and Mod-6)
* Decoders (BCD to 7-segment)
* 7-Segment Displays
* Proteus Software to Simulate Circuit

# Methodology

## We can Generate Pulse with 555 Timer IC or we can use the digital Clock in Software: Clock Pulse Generation:

A 555 Timer IC was configured in astable mode to generate continuous clock pulses. These pulses act as the base timing for the digital clock.

## Counter Design:

The digital clock is built using counters to keep track of seconds, minutes, and hours. A combination of Mod-10 and Mod-6 counters were used:

* + - Seconds: 2-digit counter (00 to 59)
    - Minutes: 2-digit counter (00 to 59)
    - Hours: 2-digit counter (00 to 23 or 12, depending on format)

## Display Logic:

The outputs of the counters were decoded using BCD to 7-segment decoder ICs to drive the 7-segment displays for visual representation.

## Synchronization and Reset:

Logic gates were used to reset the counters after reaching their maximum value and to synchronize the cascading of counters from seconds to minutes to hours.

## Theoretical Calculations and Equations:

**Counter Using JK Flip-Flops:** We derived the excitation table for JK flip-flops and applied Karnaugh maps (K-maps) to simplify the required logic expressions for the toggling conditions. For a 4-bit Mod-10 counter, the flip-flop input equations were derived based on the state transitions.

Example:

* + - For Flip-Flop A: (toggles every clock pulse)
    - For Flip-Flop B:
    - Further equations were derived similarly for the remaining flip-flops.

## 7-Segment Display Decoder Logic:

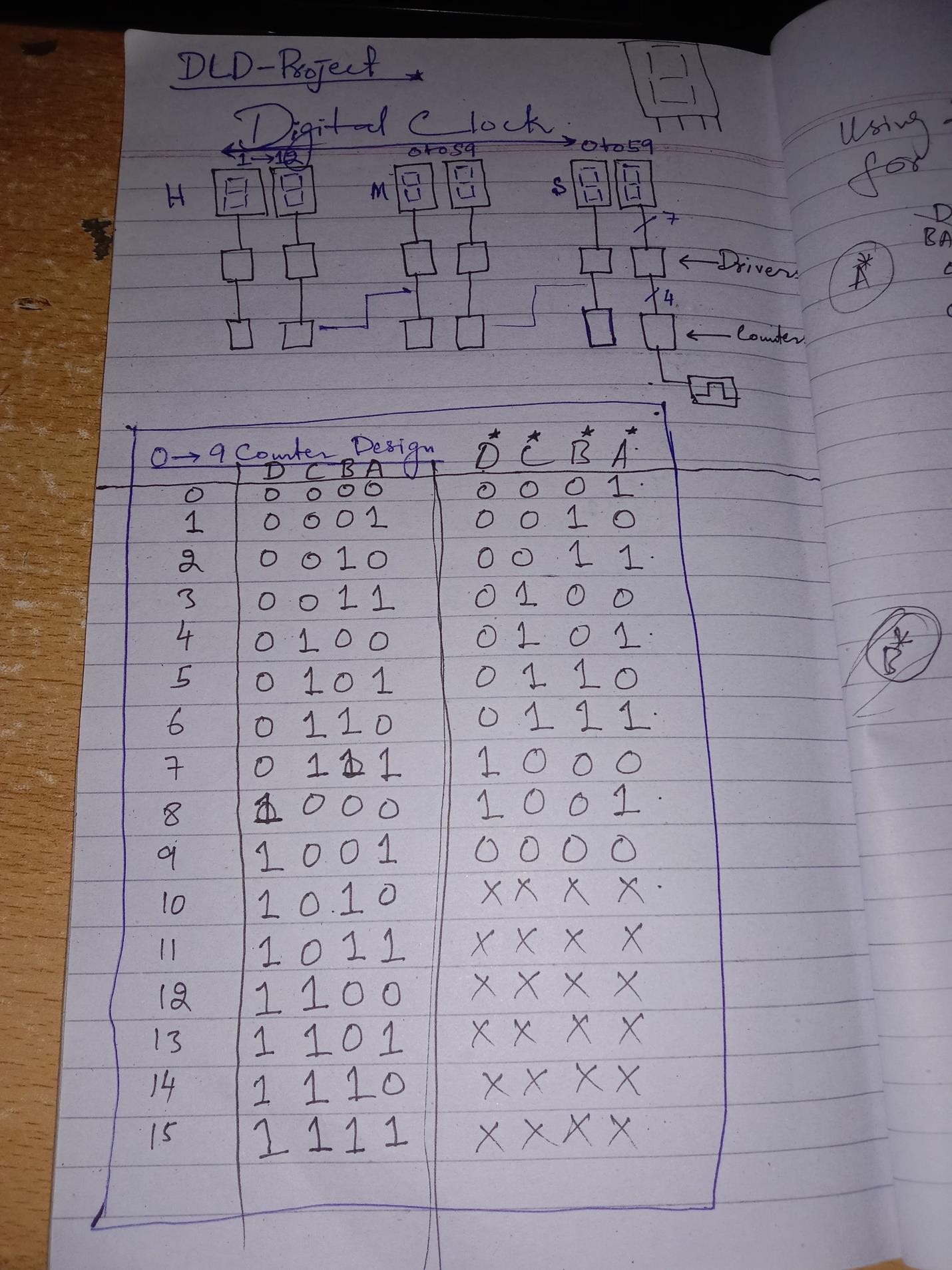
For each decimal digit (0–9), we derived the logic equations for each of the seven segments (a to g) using truth tables and K-maps.

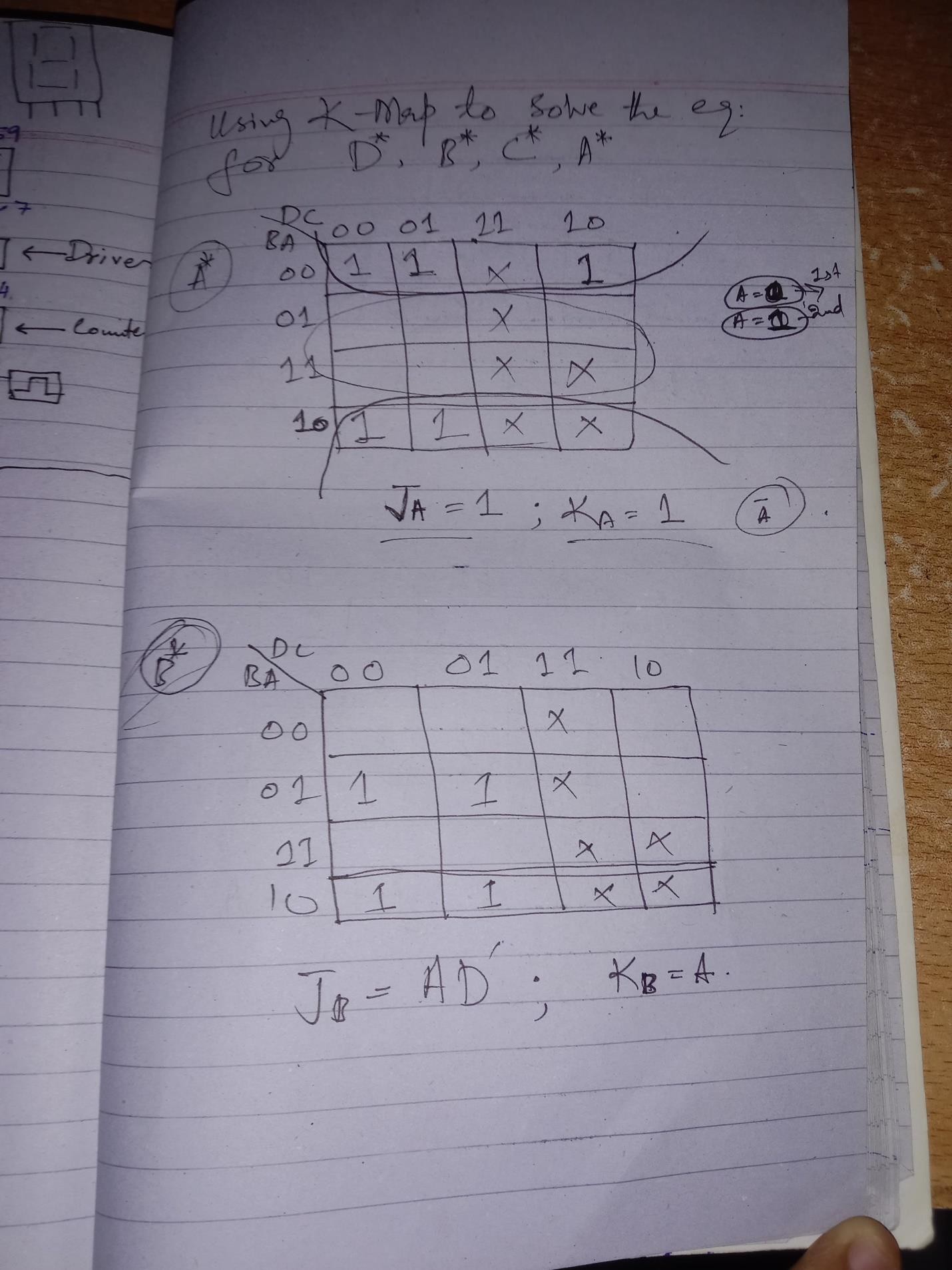
Example for segment 'a':

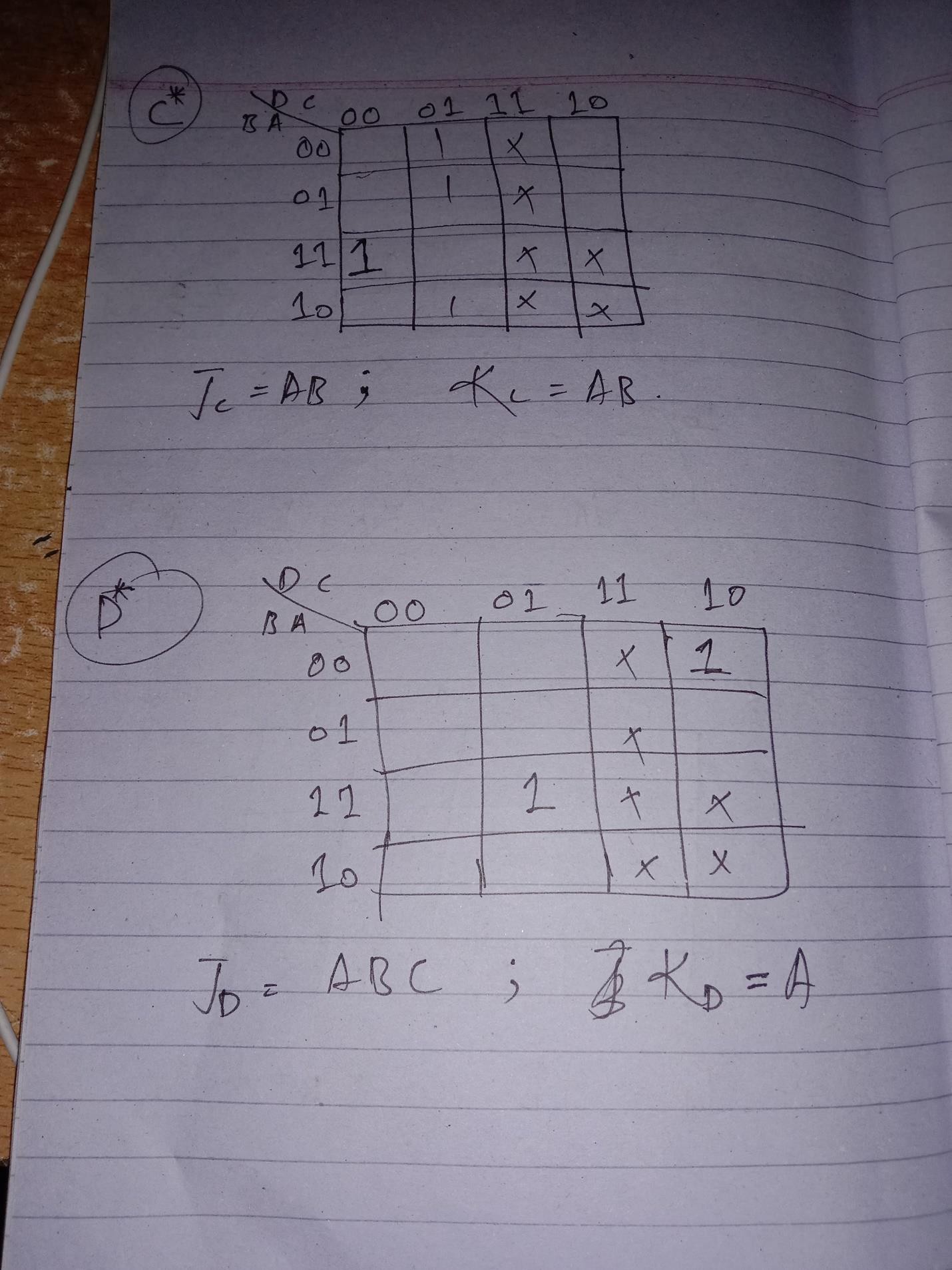
* Truth table values for BCD inputs (A, B, C, D)
* K-map simplification for segment 'a'
* Resulting minimized Boolean equation used to design logic with gates

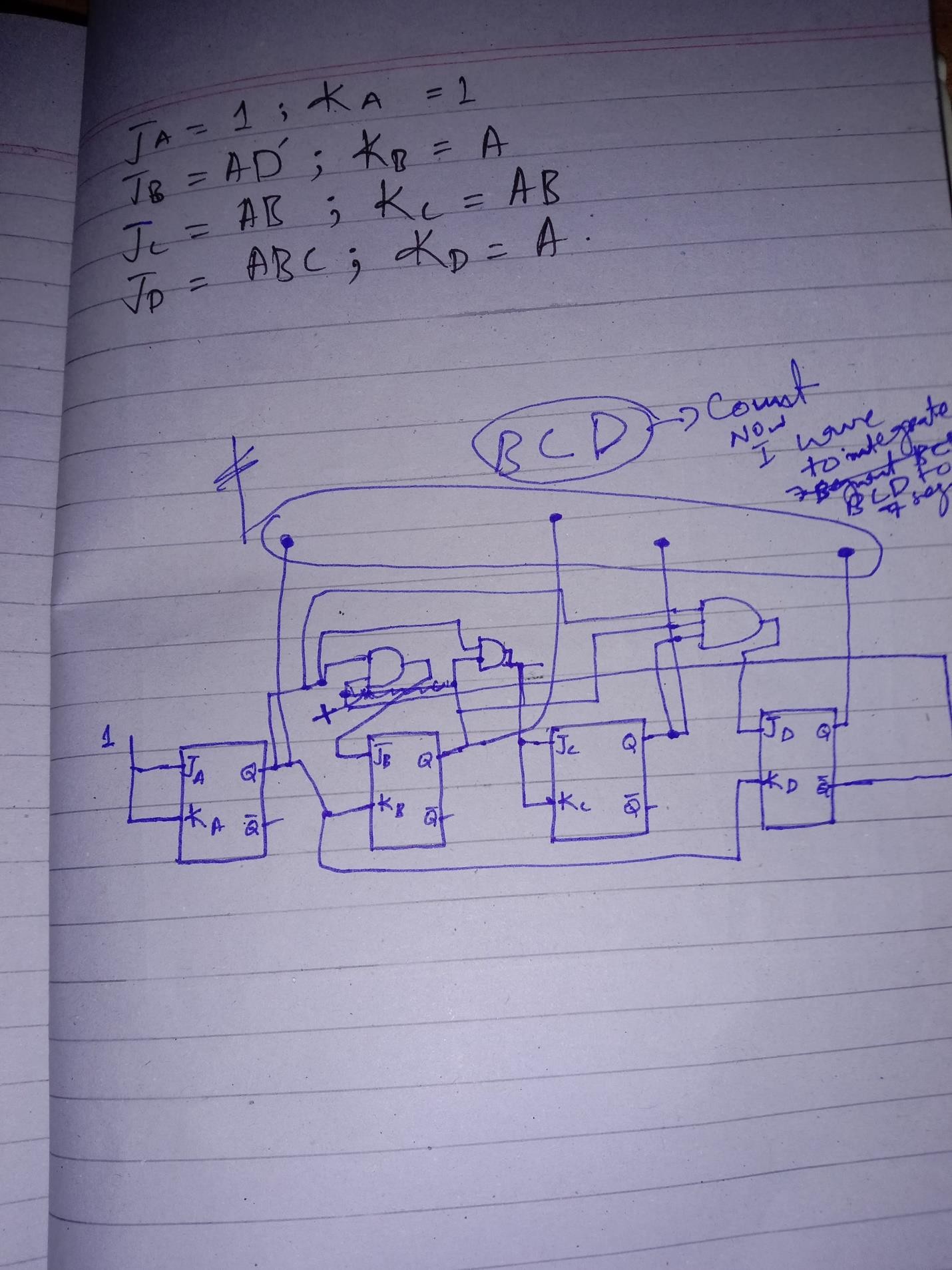
These equations were implemented using discrete logic gates, avoiding the use of dedicated decoder ICs.

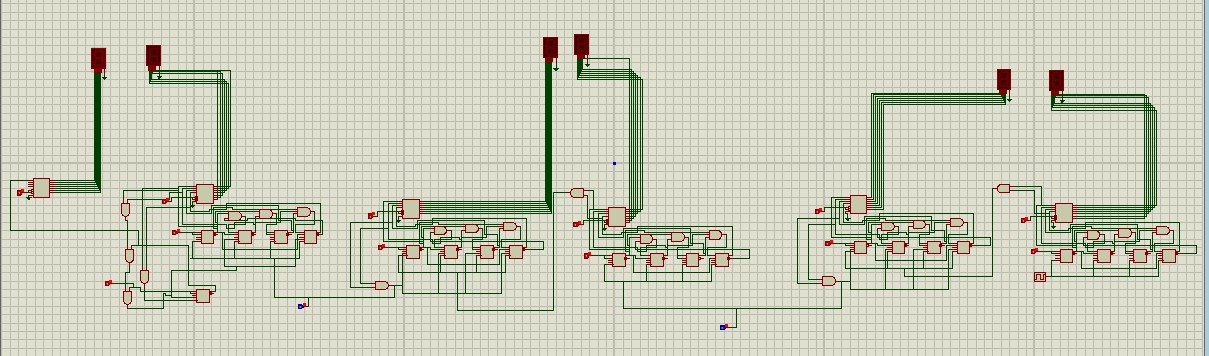
1. **Circuit Diagram** (A hand-drawn or simulated diagram should be attached here showing the connections and components.)

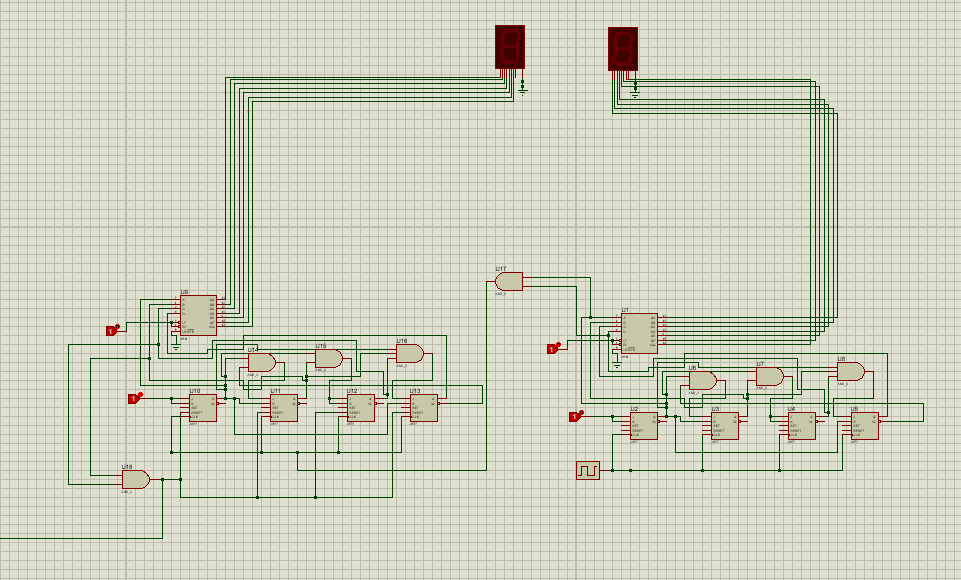


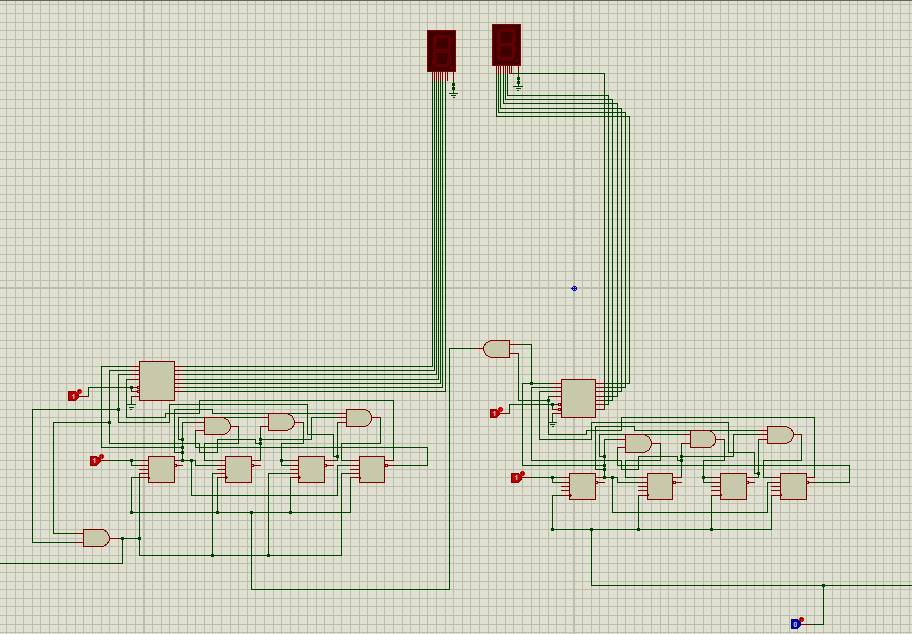


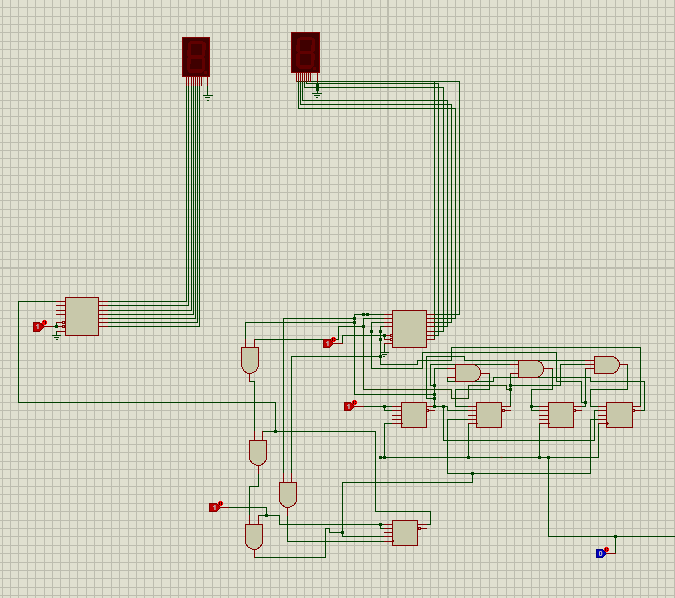


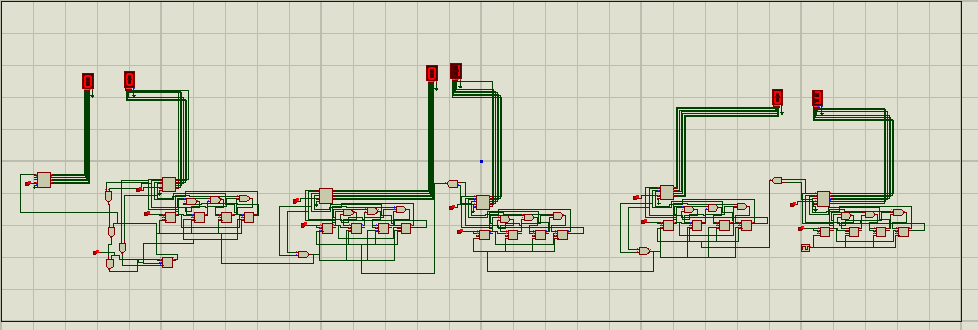


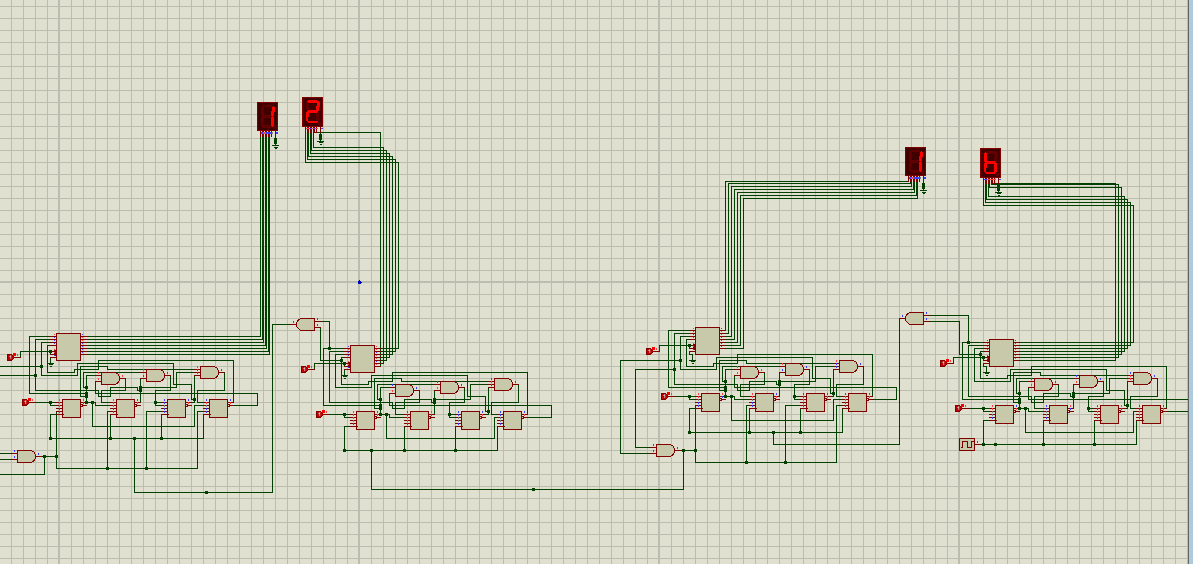
Full Circuit Scamatic:

For Second:

For Minutes:

For Hours:

Simulation:



# Results and Observations

The digital clock accurately displayed the time in HH:MM:SS format. The transitions between counters occurred smoothly, and the displays updated in real-time. Minor issues in initial synchronization were fixed by adjusting the logic gate connections and reset conditions.

# Challenges Faced

* Ensuring accurate pulse generation and timing.
* Synchronizing multiple counters.
* Designing minimized logic for display decoder manually
* Debugging incorrect counter states due to JK flip-flop miswiring

# Conclusion

The project successfully demonstrated the design and implementation of a digital clock using basic logic gates and sequential circuits. It reinforced theoretical knowledge of digital electronics and improved practical skills in circuit building and debugging.

# References

* Digital Design by M. Morris Mano
* Class Lecture Notes
* Online Electronics Forums and Tutorials
* K-map and Boolean Algebra Reference Sheets